ITk Strip Electronics Activities at UC Santa Cruz: Data Transmission, ASIC Design

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Overview of UCSC Electronics Activity

- Tight focus on critical items
- R&D on electrical data transmission along stave
  - Point-to-point data transmission at 640 Mbps
  - Multi-drop clock/command transmission at 160 Mbps
  - Transmission protocols and signal conditioning
  - No construction responsibilities here; complete R&D for final strip detector design in 2016 (needs to be finished for TDR)
- ASIC design for strip detector readout
  - Functional block design for ABC/HCC chip families
  - Testbench simulation code for ABC/HCC verification
  - Sample driver designs for low-power signaling
  - This critical-path design work will need to continue for the next few years

Data Transmission R&D

- #1 on the "top-10" priority list from Strip Project Leaders: *"Can we count on 640 Mbps data transmission on long flex tapes?"*
  - Point-to-point transmission on dedicated differential striplines
  - Data rate from hybrids is set by the 1 MHz readout spec
  - How do extremely long flex tapes (1.4 m) behave when sandwiched between silicon strip sensors and carbon fiber stave?
  - What additional signal conditioning is required? (8b/10b, pre-emphasis)

- Is multi-drop transmission of 160 Mbps clock and command possible with so many hybrids?
  - What special considerations are needed for receivers on the hybrids?
  - What is the acceptable bit error rate on the command lines?

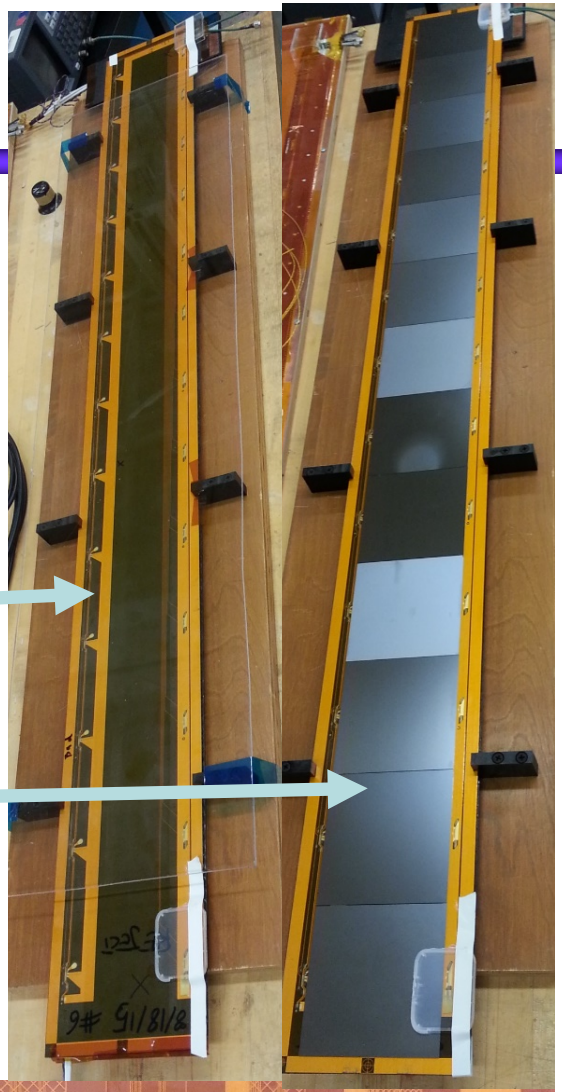
- We were asked to work on DAT by Strip Project Leaders, due to special expertise. This work must converge soon! (before TDR)

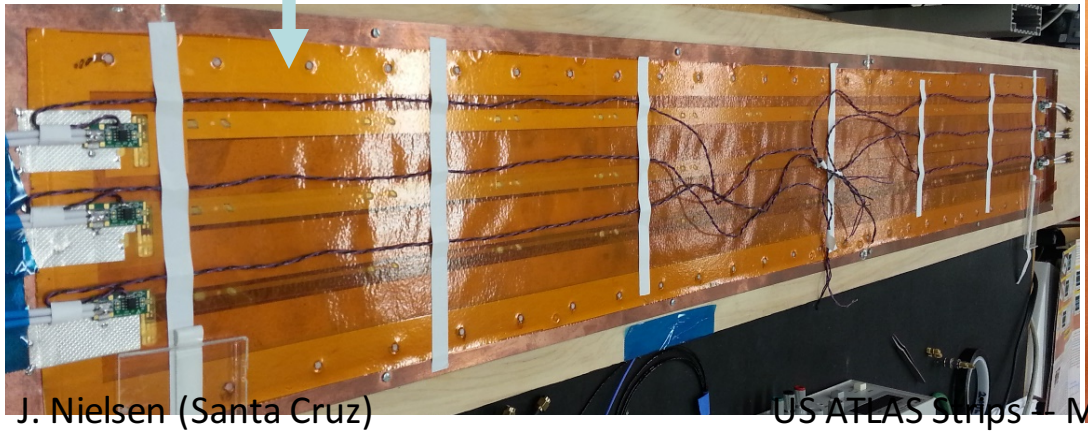
Point-to-Point Transmission at 640 Mbps

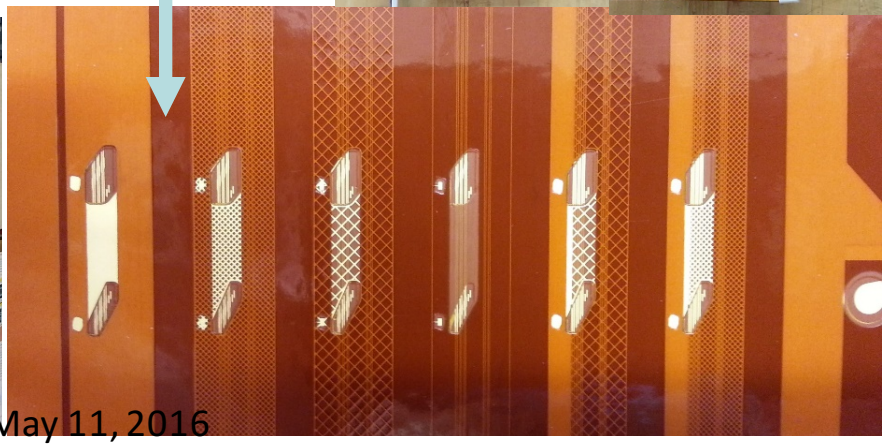
- Major R&D involving shield planes embedded in tape or stave
  - Bottom shield: current carbon fiber thickness seems insufficient; need additional metal layer on tape to provide conductive shield
  - Top shield: sensors have ~100 nm of backside metallization
- Test different shielding strategies, together with prototype stave
  - Mock-up mounted on thick copper baseplate delivered bandwidth significantly above 640 Mbps, even without 8b/10b encoding or pre-emphasis
- Plan to test new tape incorporating our design feedback
- Need to evaluate bandwidth measurements and bit-error rate using new HCC test drivers from Penn

Bus Tape Prototypes

Tape	Length	Track / Gap	Bottom surface	Top shield/surface
Old test tape	126 cm	130-140 um / 150-160 um	Copper surface	Full/partial /no shield
Full layout without sensors	~125 cm	87-93 um / 102-114 um	Carbon fiber	None
Full layout with sensors	~125 cm	87-93 um / 102-114 um	Carbon fiber	Sensors
New test tape	132 cm	Varying	Copper shield	6 variants

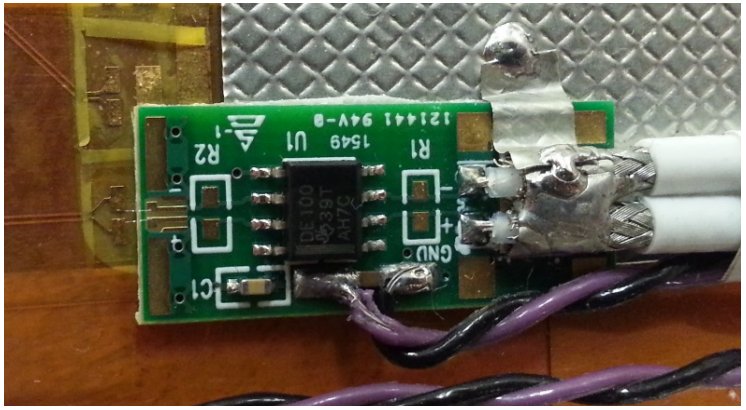






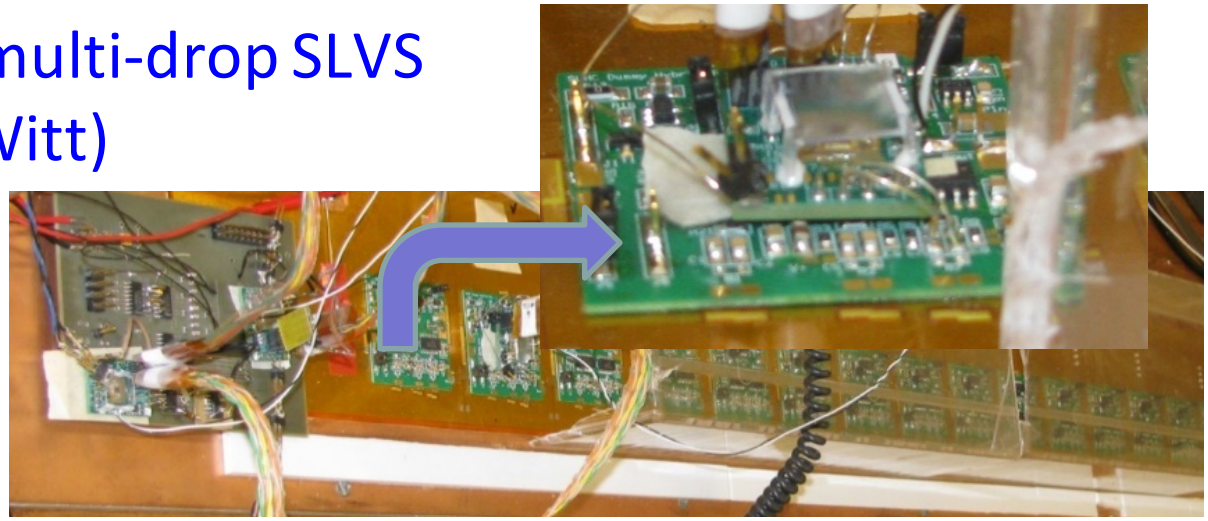
Test Equipment at SCIPP

- Each tested tape link had driver and receiver on the ends. They were connected to coaxial lines going to/from BERT systems.



Coax from BERT | Driver | Tape | Receiver | Coax to BERT

- Dedicated transceiver for multi-drop SLVS studies: AUEIO chip (J. DeWitt)



Measurements at 640 Mbps

- Point-to-point links in newest bus tape are mostly unshielded, but impedance is still uniform, matches 100 Ω
  - Determined with TDR measurements

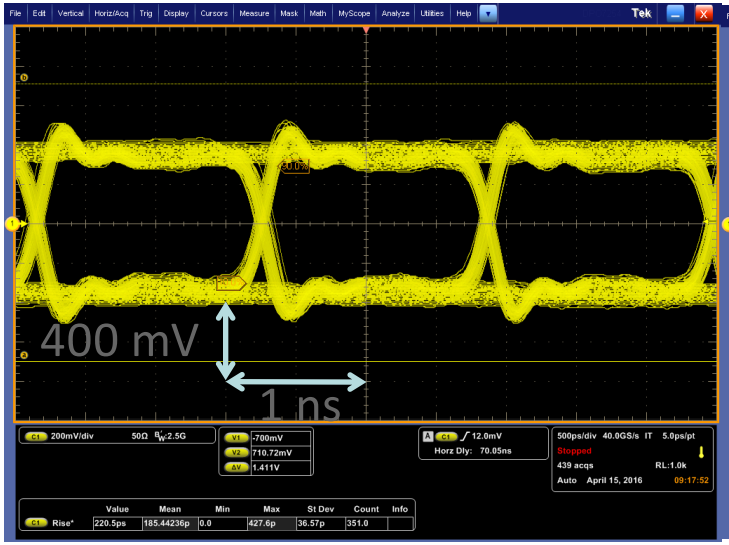
Top	Impedance
None	99.6 +/- 0.8 Ω
Sensors	95.6 +/- 0.3 Ω

- Results on new tape (co-cured with carbon fiber) not as good as old tape (copper baseplate), due to resistive losses in carbon fiber

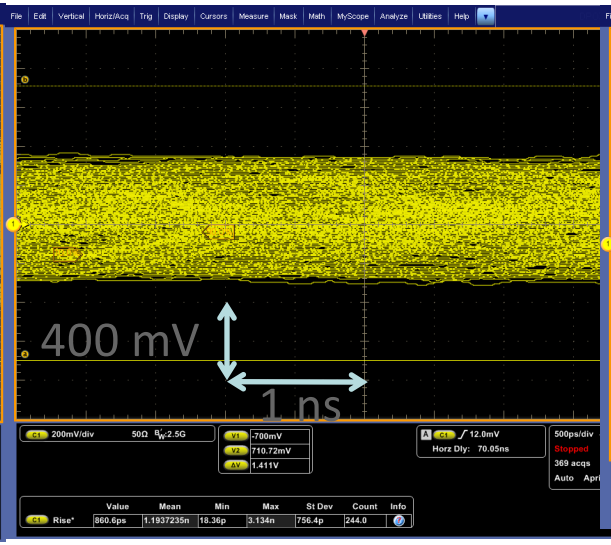
Line type	8/10 b?	Pre-emphasis?	TX BW [Gbps]	Payload BW [Gbps]	Error Rate
Old tape (full shield)	No	No	0.777	0.777	9.04e-14
	Yes	No	1.244	0.995	< 1.39e-14
New tape (with sensors mounted)	No	No	< 0.622	< 0.622	
	Yes	No	< 0.622	< 0.622	

Measurements at 640 Mbps

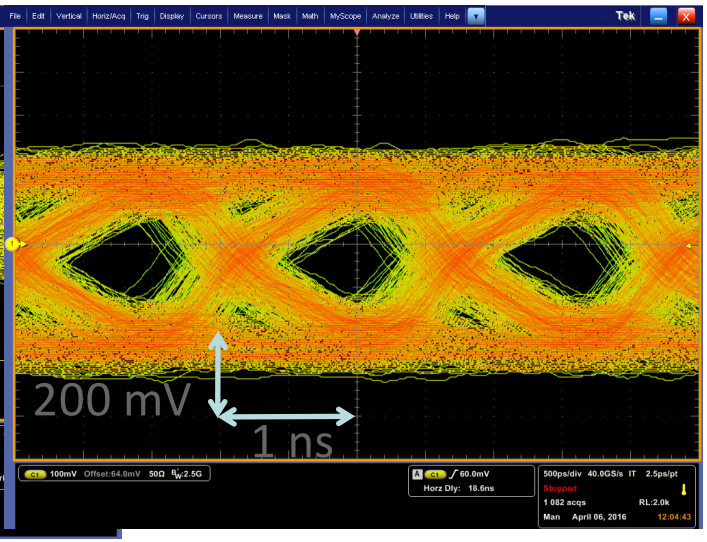
Tape input (post-driver)



Tape output on CaF

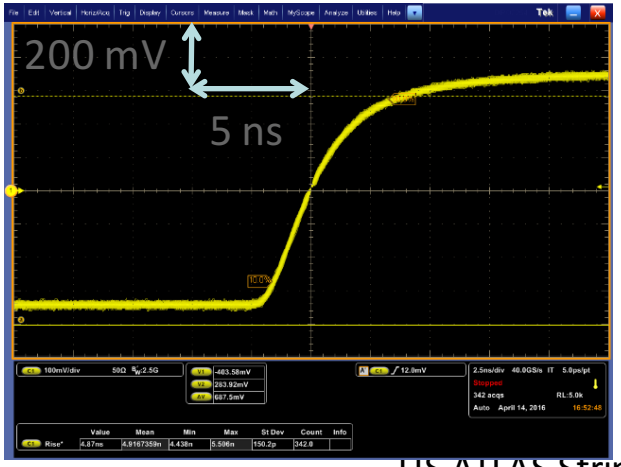


Tape output on copper

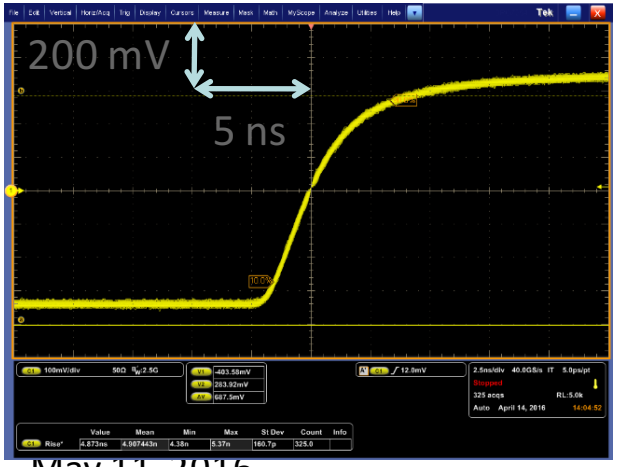


- Rise times on order of 5 ns (too long); may need pre-emphasis

No sensors

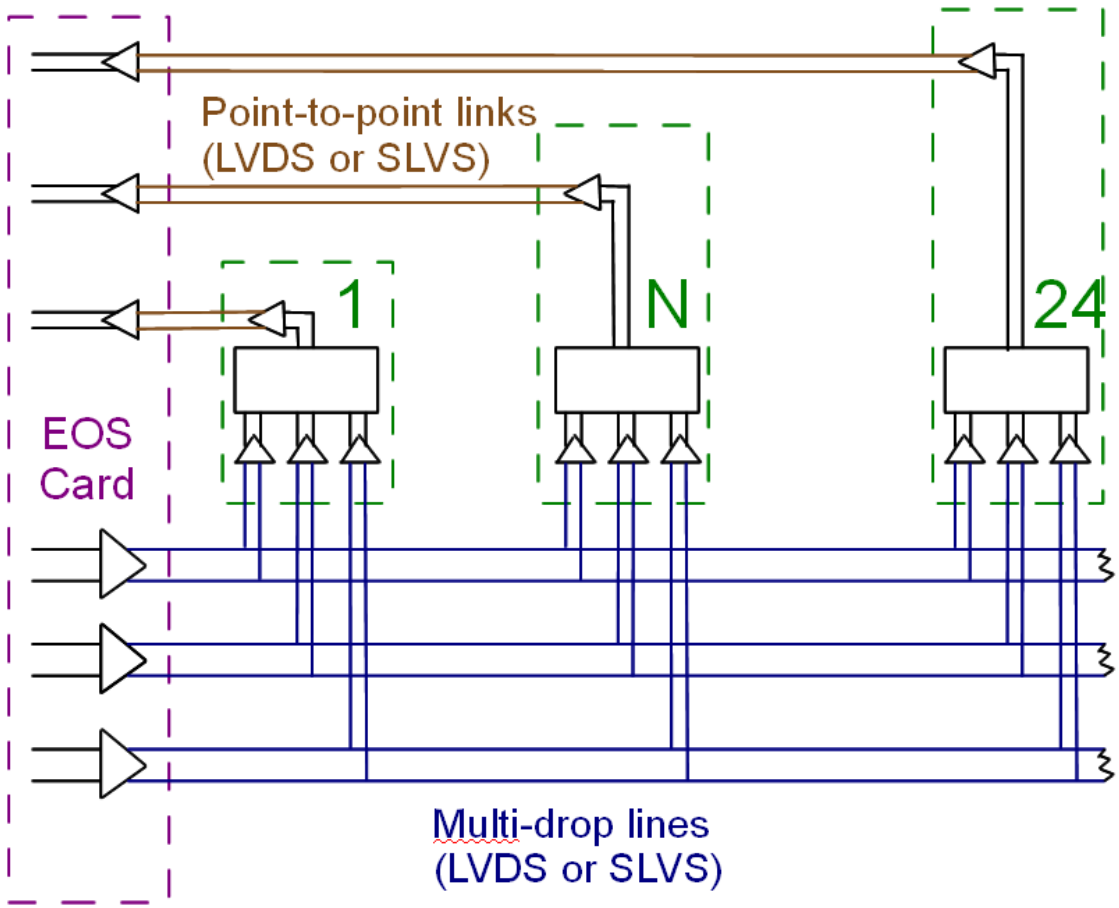


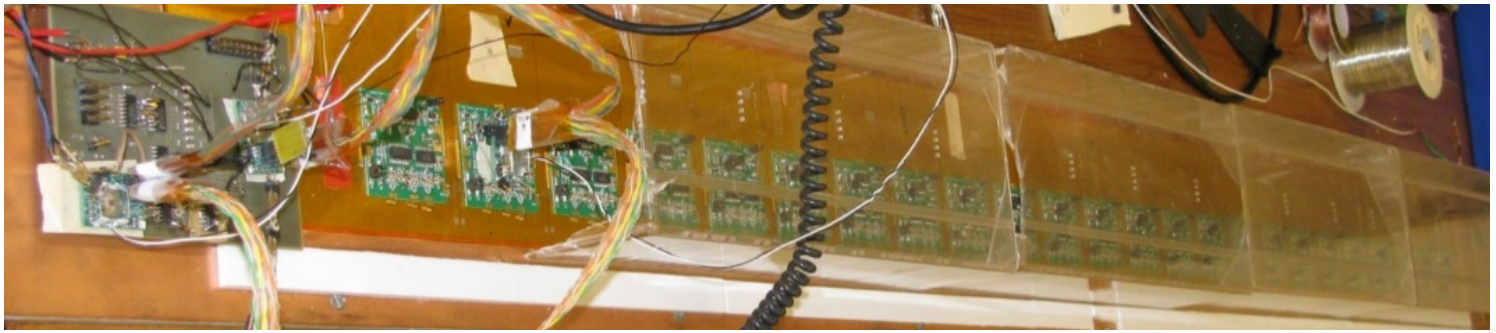
With sensors



Multi-drop Transmission at 160 Mbps

- Loop-back test setup
  - Commercial buffers represent hybrid endpoints
  - But replace some "hybrids" with AUEIO chips to test SLVS protocol
- Tests of older tape demonstrated error rate less than 10^{-12} for signal amplitudes larger than 100 mV





ASIC Design Development

- Designer Joel DeWitt has been part of the design team for the ITk Strip Readout ABC/HCC chip set since the beginning
- Very close collaboration with the Penn and CERN IC designers
- For the first prototypes of ABC130 & HCC130, he developed the original testbench simulation code to verify the ABC/HCC interactions in addition to other circuit blocks such as the command decoder.
- For the ABC* now in development, he has designed at least 12 circuit blocks including the top-level command decoder and read-out module, and the readout serializer.
- As the logic blocks of the ABC* are completed, Joel will switch his attention to help Penn with the design of the HCC*.

Summary from UCSC

Data Transmission

- Deliverables (from R&D efforts only, no construction):
  - High-speed bit-error rate testing of prototype bus tapes with realistic grounding and shielding conditions
  - Feedback on bus tape layout, stave facing design, communications protocols
- People involved: V. Fadeyev, A. Grillo, F. Martinez-McKinney, J. Nielsen, undergrads
- Dependence on resources outside U.S.:
  - Long stave bus tapes are designed by collaborators in UK (Oxford/RAL)

ASIC Design

- People involved: J. DeWitt
- Current efforts: functional blocks for ABC* and HCC* designs
- Anticipated timeline: design schedule for ABC* and HCC*